forming the N-type coupling region **107** after conducting the ion implantation over the first N-type buried region **106** and the second N-type buried region **108**. Preferable range of the impurity concentration and/or the formation region for the first N-type buried region **106**, the N-type coupling region **107** and the second N-type buried region **108** in this case may be similar to that described above.

SECOND EMBODIMENT

[**0077**] In the present embodiment, the semiconductor device **100** further includes a preventing region, which is formed between the N-type coupling region **107** and the P-type base region **112**, and is capable of preventing a broadening of the P-type base region **112**. Having such configuration, even if the effective base region **112'** is broadened during the operation of the transistor Q_1, the broadening thereof in the transverse direction can be prevented by the preventing region. Having this configuration, even though the P-type base region **112** and the N-type coupling region **107** are arranged in relatively closed positions, an electrical current flows through N-type coupling region **107** when a larger electrical current flows to the N-type emitter region **114** from the N-type collector region **118**, and therefore an impact ionization is generated in the N-type coupling region **107**.

[**0078**] **FIGS. 12A and 12B** are diagrams, showing a configuration of the semiconductor device **100** in the present embodiment. **FIG. 12A** represents a cross-sectional view, and **FIG. 12B** represents a schematic plan view. The semiconductor device **100** further includes an insulating separating portion **122**, in addition to the configuration described in first embodiment in reference to **FIG. 1**. The insulating separating portion **122** is formed by forming a splitting trench between the N-type coupling region **107** and the P-type base region **112**, and plugging the splitting trench with an insulating material.

[**0079**] Having this configuration, the position for forming the N-type coupling region **107** can be determined without considering the broadening of the effective base region **112'** during the operation of the transistor Q_1. Therefore, the semiconductor device **100** can be miniaturized.

[**0080**] **FIGS. 13A and 13B** are diagrams, showing other configuration of an insulating separating portion **122**. **FIG. 13A** represents a cross-sectional view, and **FIG. 13B** represents a schematic plan view. As such, even if the configuration of surrounding the P-type base region **112** with the insulating separating portion **122** is presented, the broadening of the effective base region **112'** during the operation of the transistor Q_1 can be prevented, and therefore a contact of the effective base region **112'** with the first N-type buried region **106** can be prevented.

[**0081**] **FIGS. 14A and 14B** are diagrams, showing other configuration of an insulating separating portion **122**. **FIG. 14A** represents a cross-sectional view, and **FIG. 14B** represents a schematic plan view. As such, even if the configuration of surrounding the N-type coupling region **107** and the first N-type buried region **106** with the insulating separating portion **122** is presented, the broadening of the effective base region **112'** during the operation of the transistor Q_1 can be prevented, and therefore a contact of the effective base region **112'** with the first N-type buried region **106** can be prevented.

[**0082**] **FIGS. 15A and 15B** are diagrams, showing other configuration of an insulating separating portion **122**. **FIG. 15A** represents a cross-sectional view, and **FIG. 15B** represents a schematic plan view. As such, even if the configuration of dividing and surrounding the P-type base region **112**, and the N-type coupling region **107** and the first N-type buried region **106** with the first insulating separating portion **122***a* and the second insulating separating portion **122***b* is presented, the broadening of the effective base region **112'** during the operation of the transistor Q_1 can be prevented, and therefore a contact of the effective base region **112'** with the first N-type buried region **106** can be prevented.

[**0083**] **FIG. 16** is a cross-sectional view, showing other example of the semiconductor device **100** in the present embodiment. In this case, the semiconductor device **100** has an N-type region for isolation **109**, in place of the insulating separating portion **122** shown in **FIG. 12A**. In this case, an exemplary case of forming the N-type region for isolation **109** as having a depth that reaches the second N-type buried region **108** is illustrated. The N-type region for an isolation **109** can be formed by an ion implantation, simultaneously with forming the N-type collector region **118**. Having this configuration, the position for forming the N-type coupling region **107** can be determined without considering the broadening of the effective base region **112'** during the operation of the transistor Q_1. Therefore, the semiconductor device **100** can be miniaturized.

[**0084**] Further, N-type region for isolation **109** can also be formed to have a depth, which is shallower than the N-type collector region **118** and does not reach the second N-type buried region **108**. Having such configuration, the broadening of the effective base region **112'** during the operation of the transistor Q_1 can be prevented. This can provide miniaturization of the semiconductor device **100**.

THIRD EMBODIMENT

[**0085**] **FIG. 17** is a cross-sectional view, showing a configuration of the semiconductor device in the present embodiment. The form has been described in first embodiment and second embodiment, in which a buried region formed between the P-type substrate **102** and the N-type drift region **110** is divided into the first N-type buried region **106** and the second N-type buried region **108**, and the N-type coupling region **107** is formed therebetween. In the present embodiment, the semiconductor device **100** includes the N-type buried region **105**, instead of the first N-type buried region **106** and the second N-type buried region **108**. Further, the N-type coupling region **107** is formed between the N-type collector region **118** and the N-type buried region **105**.

[**0086**] Having such configuration, an electrical current flows through N-type coupling region **107** when a larger electrical current flows to the N-type emitter region **114** from the N-type collector region **118** during the operation of the transistor Q_1, and therefore an impact ionization is generated in the N-type coupling region **107**. This provides advantageous effects similar to that described in first embodiment.

[**0087**] Concerning the N-type coupling region **107**, an N-type diffusion layer is formed on the surface of the N-type drift region **110** by, for example, an ion implantation, and thereafter, such N-type diffusion layer is diffused into the